Product Brief

Universal Multiport Memory Controller (UMMC)

Overview

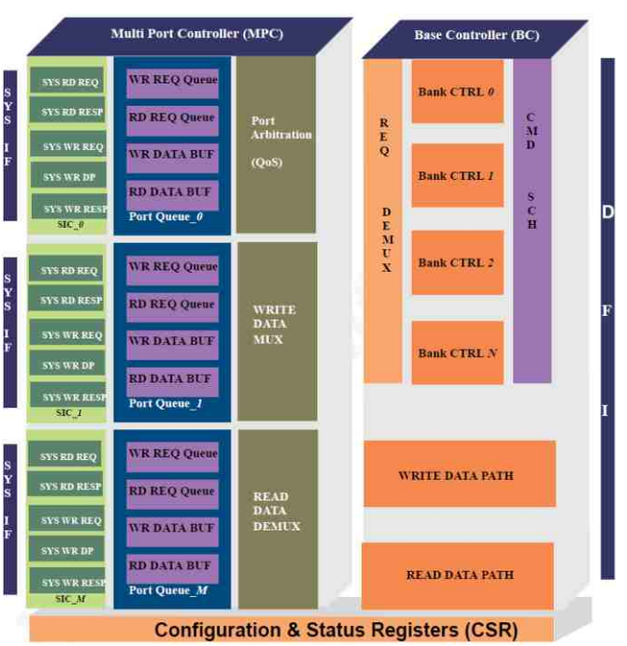
Mobiveil's UMMC Controller is a highly flexible and configurable design. It is targeted for high bandwidth access and low power consumption such as next-generation mobile, networking and consumer applications. The controller architecture is carefully tailored to achieve reliable high-frequency operation with dynamic power management and rapid system debug capabilities.

UMMC Controller is part of Mobiveil's Storage and Memory controller family of IP solutions which also includes DDR4/3, NVM Express (UNEX), Integrated Flash Controller (IFC), and Secured Digital Host Controller (eSDHC) IP cores.

The controller's configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible AXI System interface makes it easy to be integrated into wide range of applications. UMMC controller leverages Mobiveil's years of experience in HyperTransport, PCI, PCIe and RapidIO technologies and in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter-operability.

Features

- Compliant with AXI V1.0 specification
- Compliant with DFI 3.1 specification
- Compliant with JEDEC LPDDR2 and LPDDR3 standards
- Support for 8, 16, 32 SDRAM bus width, for a total memory data path width up to 64 bits
- Supports chip select interleaving
- Supports single and multi-port host buses AMBA 3 AXI up to 32 ports



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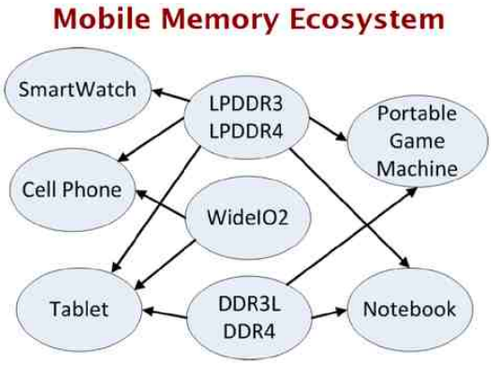

Configrable options

- Configurable AXI address width
- Configurable Request queue depth
- Configurable Write and Read data FIFO size
- Configurable QoS through various arbitration schemes

- Status : Silver
- Availability : Contact ip@mobiveil.com
- Language : Verilog
- Synthesis : Synopsys DC, Synplify-Pro
- Simulation : Cadence, Synopsys, Mentor
- Technology : 90nm ASIC or better, FPGA

About Mobiveil

Mobiveil is a fast growing Technology company that specializes in creation of Intellectual Properties, Frameworks and Solutions for the Networking, Enterprise and Device Mobility markets. The Mobiveil team leverages decades of experience in delivering high-quality, production-proven, high-speed serial interconnect Silicon IP cores to the leading customers worldwide. With a highly motivated engineering team, dedicated integration support, flexible business models, strong industry presence through strategic alliances and key partnerships, Mobiveil solutions have added tremendous value to the customers in executing their marketing and engineering goals within budget and on time.

Mobiveil is headquartered in the Silicon Valley with engineering development centers located in Milpitas,CA, Chennai and Bangalore, India, and sales offices and representatives located in US, Europe, Israel, Japan, Taiwan and Peoples Republic of China.

Specifications

Features

- Support for up to four ranks (chip selects) and 4/8 banks per rank (chip select)
- Supports MC Clock to PHY Clock ratio in Full/Half/Quarter rate mode
- Supports Auto-refresh, per bank refresh, self-refresh, power-down, and deep power down modes
- Maximizes bus efficiency through look-Ahead command processing, bank level parallelism and intelligent request scheduling
- Built-in asynchronous interface support for DRAM frequencies that are not equal to the AXI frequency
- Separate write and read queues
- The AXI ID signals support out-of-order transactions

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

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