Mobiveil RapidIO to AXI Bridge Controller (RAB)

Overview Features

PRODUCT BRIEF

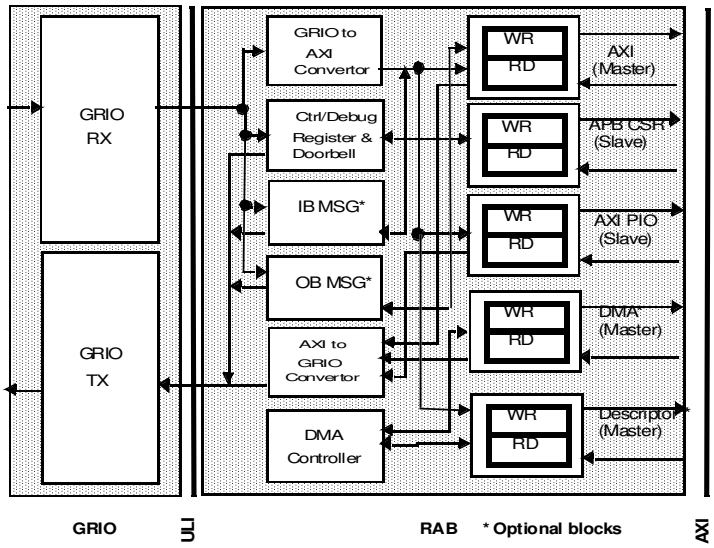
Highly Configurable
Technology Independent
System Validated

Mobiveil's RapidIO-AXI Bridge (RIO-AXI Bridge) is a highly flexible and configurable IP used along with Mobiveil native RapidIO Controller (GRIO) to provide RapidIO interface on one side and AXI interface on the system side. The Bridge has been architectured to interface with a RapidIO controller used as a Host or device. The RIO-AXI BRIDGE uses high speed multi-channel DMA and Message controllers to match the bandwidth requirements of the RIO solution.

The Mobiveil RIO-AXI Bridge is a simple, configurable and layered architecture, independent of applications, implementation tools or target technology. The controller architecture is carefully tailored to optimize latency, power consumption, and silicon footprint, making it ideal for cost and performance sensitive applications. The RIO-AXI BRIDGE solution provides highly scalable bandwidth through a configurable data path width and clock frequency.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

- Compliant with RapidIO specification, Revision 2.2
- Compliant to AMBA AXI protocol v1.0
- Supports 32-bit or 38-bit addressing
- AXI PIO operation with configurable number of AXI Slaves
- RapidIO PIO operation with configurable number of AXI Masters
- Multi-channel Read and Write DMA
- Register based and descriptor based modes of DMA
- Interrupt generation to both AXI and RapidIO
- Inbound and Outbound Doorbell
- Logical Flow control
- Bypass Mode
- Software configurable address mapping between RapidIO and AXI systems
- CSR registers optional access through APB
- Inbound and Outbound Mailbox Support
- Data streaming support
- Supports 64 and 128 bit Datapath



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Status	**Gold**
Availability	**Available**
Language	**Verilog**
Synthesis	**Quartus**
Simulation	**Cadence, Synopsys, Mentor**
Technology	**Altera Stratix, Arria, Cyclone FPGA**

Specifications

Configurable Options

- PIO, DMA, Message, Data streaming or mixed mode of operation
- Up to 8 Read and Write DMA Channels
- Up to 8 RapidIO capable AXI Slave PIO devices
- Up to 8 AXI capable RapidIO devices
- Maximum DMA transfer size of 1 MB
- Register based or Chain Descriptor based DMA types
- Priority level transaction initiations by different DMA/PIO devices
- Programmable address mapping for PIO transfers
- RapidIO or AMBA hosted DMA accesses

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

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