Mobiveil RapidIO Controller (GRIO™)

Overview

Mobiveil's RapidIO Controller solution (GRIO™) is a highly flexible and configurable IP. The Mobiveil RapidIO Controller Solution can be used as a Host or device. The RapidIO Controller when used along with Mobiveil's RapidIO to AXI Bridge (RAB) provides high speed multi-channel DMA, Data Message and Data streaming functionality to match the bandwidth requirements of the RapidIO interface.

The Mobiveil RapidIO Controller has a simple, configurable and layered architecture, independent of applications, implementation tools, PHY Designs or most importantly target technology. The controller architecture is carefully tailored to optimize latency, power consumption, and silicon footprint, making it ideal for cost and performance sensitive applications. The RapidIO solution provides highly scalable bandwidth through a configurable data path width and clock frequency.

Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

Features

- Compliant to RapidIO Specifications revision 3.0
- Compliant with RapidIO Error Management Extension specification, Revision 3.0
- Implements Logical, Transport and Physical layers functions
- Architected for high link utilization and low latency
- Efficient receive and transmit buffering scheme
- Implements receiver controlled flow control
- Provides Packet oriented user logic interface
- Serial and Parallel interfaces supported
- 1x, 4x,8x and 16x serial interface and 8 and 16 bits parallel interface
- 64/128/256-bit internal data path
- PBUS interface for configuration register access
- Up to 256 Bytes data payload
- Hardware error recovery
- Exhaustive error reporting and handling
- Pass-Through mode of operation for RIO packets up to 288 bytes
- Accept all Mode of operation for fail over support

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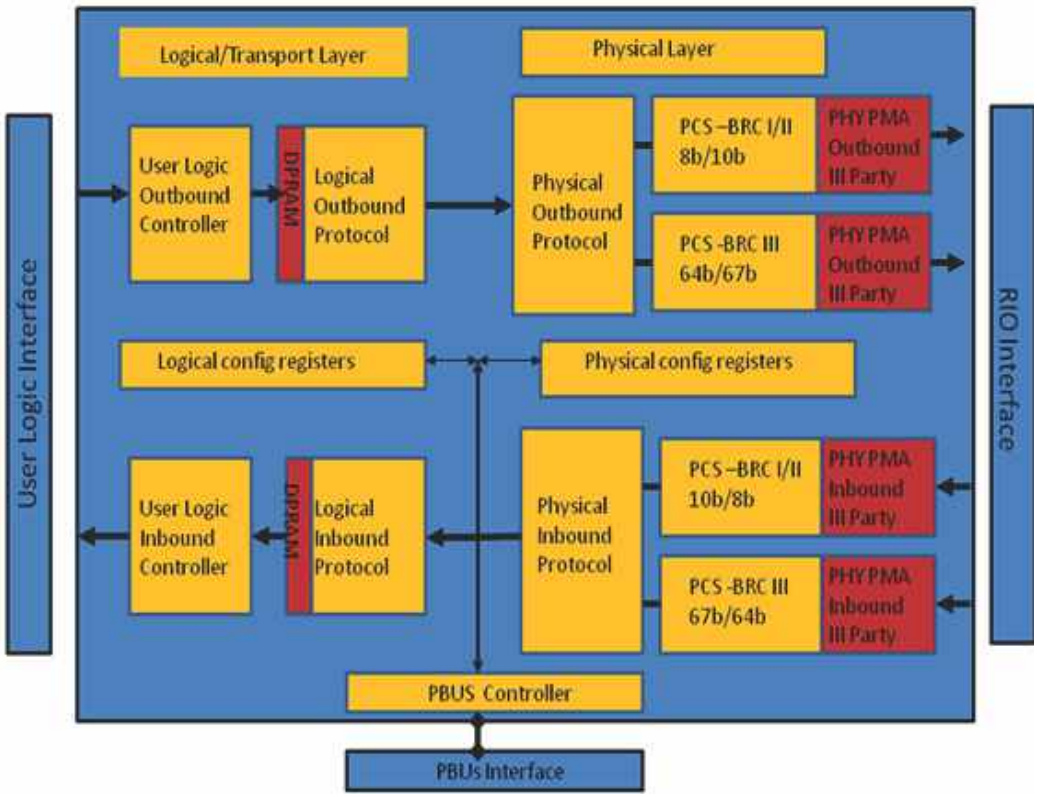

- Status : Gold (Gen1 and Gen2)
- Availability : Available
- Language : Verilog
- Synthesis : Synopsys DC, Synplicity
- Simulation : Cadence, Synopsys, Mentor
- Technology : 90nm ASIC or better, FPGA

Specifications

Configurable Options

- PIO, DMA, Message, Data streaming or mixed mode of operation
- Parallel/Serial mode of operation
- Bypass Support

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug

Product Package

- Configurable RTL Code
- HVL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

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