Gen3 PCIe to AXI Bridge (GPEX-AXI)

PCI EXPRESS

PRODUCT BRIEF

Overview

Highly Configurable
Technology Independent
System Validated

Mobiveil's GPEX with AXI Bridge (PCIe to AXI Bridge) is a highly flexible and configurable IP with a PCI Express* interface on one side and an AMBA AXI interface on the system side. The Bridge has been architectured to interface with a PCI Express* controller used as an end-point or root-complex type devices. The GPEX-AXI Bridge uses high speed multi-channel DMA controllers to match the bandwidth requirements of the PCIe Gen3 solution.

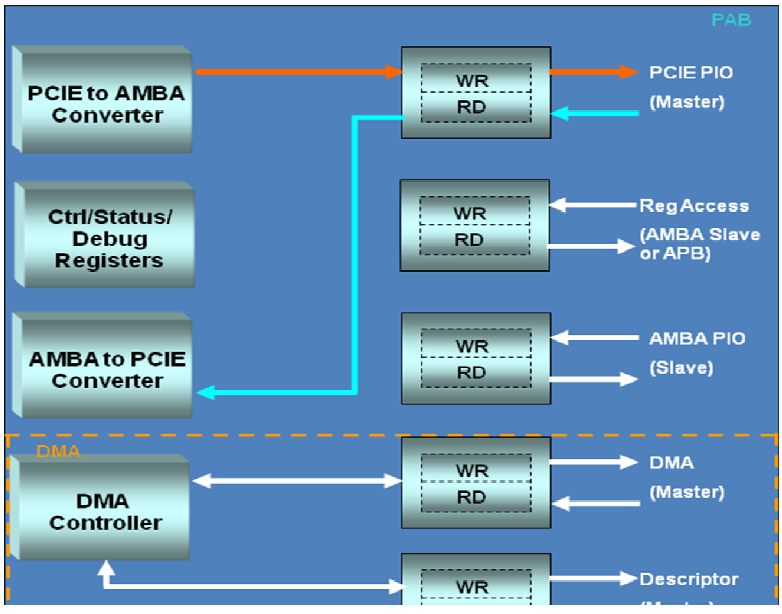
GPEX-AXI is part of Mobiveil's PCI-Express (GPEX) family of IP solutions which includes Root Complex (GPEX-RC), Hybrid (GPEX-HY), Switch port Controller (GPEX-SW), Switch (GPEX-SWITCH), GPEX-AHB Bridge (GPEX-AHB) and Advanced Switching (GPEX-AS) designs.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

GPEX-AXI leverages Mobiveil's years of experience in PCI, PCI-X and HyperTransport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability.

Features

- Compliant to PCI Express base specification version 3.0, Oct 2011 Errata for 3.0 and backward compatible with PCI Express versions 2.0 and 1
- AMBA AXI protocol 1.0 compliant
- AXI PIO operation with configurable number of AXI Slaves supported
- PCIE PIO operation with configurable number of AXI Masters supported
- Multi-channel DMA transfers supported
- Register based and descriptor based modes of DMA supported
- Read and write DMAs supported
- Interrupt generation to both AXI and PCI Express supported
- Vendor defined messages supported
- Software configurable address mapping between PCI Express and AXI systems
- Exhaustive Control, Status and Debug registers



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Status : **Gold (Gen2)**
Availability : **Available**
Language : **Verilog**
Synthesis : **Quartus**
Simulation : **Cadence, Synopsys, Mentor**
Technology : **Altera Stratix, Arria, Cyclone FPGA**

Specifications

Configurable Options

- PIO, DMA or mixed mode of operation
- Up to 8 Read and Write DMA supported
- Up to 8 PCI Express capable AXI Slave PIO devices supported
- Up to 8 AXI capable PCI Express PIO devices supported
- Maximum DMA transfer size of 1 MB
- Register based or Chain Descriptor based DMA types
- Priority level transaction initiations by different DMA/PIO devices
- Programmable address mapping for PIO transfers
- Programmable PCI Express tags reserved for each DMA/PIO device
- PCI Express or AMBA hosted DMA accesses
- AXI or APB register space accesses
- System clock frequency
- Synchronous/Asynchronous reset

Design Attributes

- Implementation specific registers for debugging
- Comprehensive error reporting
- Mailbox registers for higher layer information exchange
- Performance monitors
- Debug mode for descriptor based DMA
- Interrupt generation for debug mode events

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

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