

Gen3 PCIe Hybrid Controller with SR-IOV and ARI Support



PRODUCT BRIEF

Overview Features

Highly Configurable Technology Independent System Validated

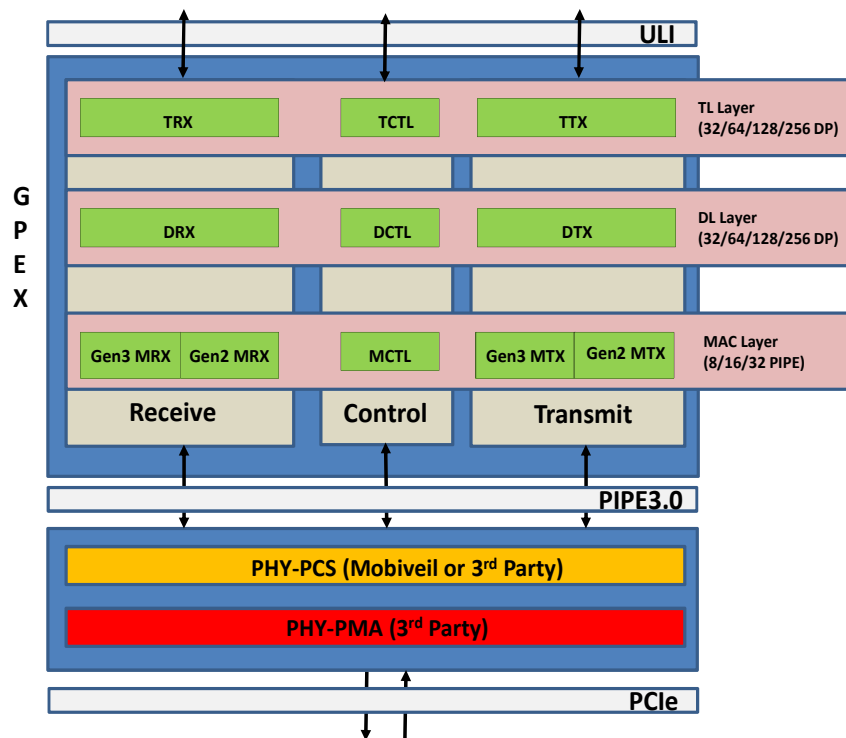
Mobiveil's PCI Express Hybrid (RC and EP) Controller is a highly flexible and configurable design targeted for end-point implementations in desktop, server, mobile, networking and telecom applications. The controller architecture is carefully tailored to optimize link utilization, latency, reliability, power consumption, and silicon footprint.

GPEX-HY is part of Mobiveil's PCI-Express (GPEX) family of IP solutions which includes Endpoint (GPEX-EP), Root Complex (GPEX-RC), Switch port Controller (GPEX-SW), Switch (GPEX-SWITCH), GPEX-AXI Bridge (GPEX-AXI), GPEX-AHB Bridge (GPEX-AHB) and Advanced Switching (GPEX-AS) designs.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

GPEX-HY leverages Mobiveil's years of experience in PCI, PCI-X and HyperTransport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability.

- Compliant to PCI Express base specification version 3.0, Oct 2011 Errata for 3.0 and backward compatible with PCI Express versions 2.0 and 1
- Supports SR-IOV and compliant to Single Root I/O Virtualization and Sharing Specification Revision 1.0
- Compliant to Address Translation Services Revision 1.0
- Supports configurable number of PFs and VFs for SR-IOV
- Architected for high link utilization and low latency
- Efficient receive and transmit-retry buffering scheme
- Completely handles PCI-Express ordering rules
- Implements flow control logic in both directions
- Packet oriented user logic interface
- Supports PIPE3.0 Compliant PHYs
- Flexible lane ordering and support for lane reversal



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Specifications

Configurable Options

- Maximum Link Width (x1, x2, x4, x8, x16)
- Maximum TLP data payload size supported (128B to 4KB)
- Data Path Widths (32, 64, 128, 256)
- Transmit Retry/Receive Buffer size
- Number of Virtual Channels
- Upstream port / downstream port
- Inclusion of specific sublayers etc.
- ASPM L1 / Wake support, Auxiliary power support
- Hot plug support

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

Status : Gold (Gen2)
Availability : Available
Language : Verilog
Synthesis : Quartus
Simulation : Cadence, Synopsys, Mentor
Technology : Altera Stratix, Arria, Cyclone FPGA

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