Quad SPI Controller

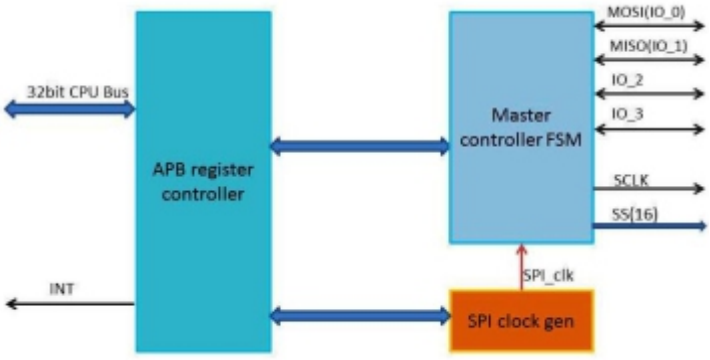
Overview

The Serial Peripheral Interface or SPI-bus is a simple 4-wire serial communications interface used by many peripheral chips that enable the controllers (SoCs' and Microcontrollers/Microprocessors) and peripheral devices to communicate with each other. The Dual/Quad SPI is an enhancement to the Standard SPI protocol (described in the Motorola M68HC11 datasheet) and provides a simple method for data exchange between a master and a slave.

Mobiveil's Quad SPI Controller is a highly flexible design using different request/response schemes and full duplex mode(standard mode) based on SPI, targeting wide variety of peripheral slave devices like ADC and DAC converters, sensors like temperature sensors and pressure sensors, or devices like signal-mixer, LCD controller, UART, CAN controller, USB controller and amplifier...etc. Also it supports serial flash memory devices from vendors like spansion, winbond etc. This controller uses 32 bit processor interface AMBA APB to support highest level of programmability.

Features

- Configurable SPI modes:
  - Standard SPI mode
  - Dual SPI mode
  - Quad SPI mode
- Standard/Dual/Quad SPI mode supports:
  - Single Master mode only
  - MSB first only
- Supports programmable SPI clocking modes
- Programmable interrupt on SPI-done
- SPI Slave devices can be independently selected
- Programmable Power-down mode for Master state-machine
- Programmable SCLK frequency derived from system clock
- Configurable Data FIFO depth



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Mobiveil Inc | 920 HillView Court | #250 | Milpitas | CA 95035
PH: 408.212.9512 | f: 408.457.0406 | e: ip@mobiveil.com
www.mobiveil.com

Differentiated Features

- Programmable request/response schemes like
  - Transmit only
  - Receive only
  - Command-address-data
  - Address-data
- Supports upto 32 bits of full-duplex transfer in standard mode
- Independently programmable frame sizes for command, address and data
- Programmable idle time between command, address and data
- Register controlled slave_select assertion/de-assertion during idle time.
- State machine status register for debugging
- Supports upto 16 Slaves

Specifications

Design Attributes

- Highly modular and programmable design
- Fully synchronous design
- Software control for key features

Product Package

- RTL Code
- System Verilog/UVM based Testbench
- Test cases
- Protocol checkers and bus watchers

Documentation

- User Guide

Licensing Options

- Single Design or Multi-project license (HDL Source Code/ FPGA Netlist).

• Status	:	Silver
• Availability	:	Contact ip@mobiveil.com
• Language	:	Verilog
• Synthesis	:	Synopsys DC, Vivado, Quartus
• Simulation	:	Cadence, Synopsys, Mentor

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