Mobiveil RapidIO to AXI Bridge Controller (RAB)

Overview

Mobiveil's RapidIO-AXI Bridge (RIO-AXI Bridge) is a highly flexible and configurable IP used along with Mobiveil native RapidIO Controller (GRIIO) to provide RapidIO interface on one side and AXI interface on the system side. The Bridge has been architected to interface with a RapidIO controller used as a Host or device. The RIO-AXI BRIDGE uses high speed multi-channel DMA, Messaging and data streaming controllers to match the bandwidth requirements of the RIO solution.

The Mobiveil RIO-AXI Bridge is a simple, configurable and layered architecture, independent of applications, implementation tools or target technology. The controller architecture is carefully tailored to optimize latency, power consumption and silicon footprint, making it ideal for cost and performance sensitive applications. The RIO-AXI BRIDGE solution provides highly scalable bandwidth through a configurable data path width and clock frequency.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and most importantly the target technology. Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

Features

- Compliant with RapidIO specification, Revision 4.0
- Compliant to AMBA AXI protocol AXI3 / AXI4
- Supports 32-bit or 38-bit or 64-bit AXI addressing
- AXI PIO operation with configurable number of AXI Slaves
- RapidIO PIO operation with configurable number of AXI Masters
- Multi-channel Read and Write DMA
Status: Gold (Gen 3)
Availability: Available
Language: Verilog
Synthesis: Synopsys DC, Cadence RC, Quartus, Vivado
Simulation: Cadence, Synopsys, Mentor
Technology: 40nm ASIC or better, FPGA

Product Package
- Verilog RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation
- Design Guide
- Verification Guide
- Synthesis Guide

About Mobiveil
Mobiveil is a fast growing Technology company that specializes in creation of Intellectual Properties, platforms and Solutions for storage, networking and IOT market. The Mobiveil team leverages decades of experience in delivering high-quality, production-proven, high-speed serial interconnect Silicon IP cores to the leading customers worldwide. With a highly motivated engineering team, dedicated integration support, flexible business models, strong industry presence through strategic alliances and key partnerships, Mobiveil solutions have added tremendous value to the customers in executing their marketing and engineering goals within budget and on time.

Mobiveil is headquartered in the Silicon Valley with engineering development centers located in Milpitas, CA, Chennai, Hyderabad and Bangalore, India, and Sales offices and representatives located in US, Europe, Israel, Japan, Taiwan and Peoples Republic of China.

Specifications

Features
- Register based and descriptor based modes of DMA
- Interrupt generation to both AXI and RapidIO
- Inbound and Outbound Doorbell
- Logical Flow control
- Bypass Mode
- Software configurable address mapping between RapidIO and AXI systems
- CSR registers optional access through APB
- Inbound and Outbound Mailbox Support
- Inbound and Outbound Data streaming support
- Supports 64/128/256 bit Datapath

Configurable Options
- PIO, DMA, Message, Data streaming or mixed mode of operation
- Up to 8 Read and Write DMA Channels
- Up to 8 RapidIO capable AXI Slave PIO devices
- Up to 8 AXI capable RapidIO devices
- Maximum DMA transfer size of 1 MB
- Register based or Chain Descriptor based DMA types
- Priority level transaction initiations by different DMA/PIO devices
- Programmable address mapping for PIO transfers
- RapidIO or AMBA hosted DMA accesses
- Up to 32 Inbound data Message Controllers
- Up to 15 Multi-segment Outbound data Message controllers
- Up to 32 Inbound Data Streaming Controllers
- Up to 32 Outbound Data Streaming Controllers

Design Attributes
- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug