Overview

Mobiveil’s GPEX with AXI Bridge (PCIe® to AXI Bridge) is a highly flexible and configurable IP with a PCI Express® interface on one side and an AMBA AXI interface on the system side. The Bridge has been architected to interface with a PCI Express® controller used as an endpoint or root-complex type devices. The GPEX-AXI Bridge uses high speed multi-channel DMA controllers to match the bandwidth requirements of the PCIe® Gen5 solution.

GPEX-AXI is part of Mobiveil's PCI Express® (GPEX) family of IP solutions which includes Root Complex (GPEX-RC), Hybrid (GPEX-HY), Switch port Controller (GPEX-SW), Switch (GPEX-SWITCH), and GPEX-AHB Bridge (GPEX-AHB) designs.

The controller’s simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and most importantly, the target technology. Mobiveil solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into a wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

GPEX-AXI leverages Mobiveil’s years of experience in PCI, PCI-X and HyperTransport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability.

Features

- Built to support PCIe® base specification 5.0 (32 Gbps per lane) and backward compatible with PCIe® versions 4.0, 3.1, 2.0 and 1.1
- AMBA AXI3 and ACE-LITE compliant
- AXI PIO operation with configurable number of AXI Slaves supported
- PCIe® PIO operation with configurable number of AXI Masters supported
- Interrupt generation to both AXI and PCI Express® supported
- Vendor defined messages supported
- Software configurable address mapping between PCI Express® and AXI systems
- Exhaustive Control, Status and Debug registers
- Traditional DMA Support
  - Write DMA: There could be one or more Write DMAs that can transfer data from AXI to PCIe
  - Read DMA: There could be one or more Read DMAs that transfer data from PCIe to AXI
  - Read Descriptor: AXI Read Master to fetch descriptors from processor memory for DMA operation
  - Write Descriptor: AXI Write Master to update descriptor status into processor memory
- QDMA Support
  - Write DMA: One Write DMA that can transfer data from AXI to PCIe
  - Read DMA: One Read DMA that transfer data from PCIe to AXI
  - Descriptor Fetch and Update: Descriptor fetching from Queues in Host memory and update to Queues
Specification

Configurable Options
- PIO, DMA or mixed mode of operation
- Up to 8 Read and Write DMA supported in Traditional DMA Mode
- Up to 2K Queues when QDMA is supported
- Up to 8 PCI Express® capable AXI Slave PIO devices supported
- Up to 8 AXI capable PCI Express® PIO devices supported
- Register based or Chain Descriptor based DMA types
- Priority level transaction initiations by different DMA/PIO devices
- Programmable address mapping for PIO transfers
- Programmable PCI Express® tags reserved for each DMA/PIO device
- PCI Express® or AMBA hosted DMA accesses
- AXI or APB register space accesses
- System clock frequency
- Synchronous/Asynchronous reset

Design Attributes
- Implementation specific registers for debugging
- Comprehensive error reporting
- Mailbox registers for higher layer information exchange
- Performance monitors
- Debug mode for descriptor based DMA
- Interrupt generation for debug mode events

Product Package
- Configurable RTL Code
- UVM based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation
- Design Datasheet
- Verification Guide
- Synthesis Guide

About Mobiveil
Mobiveil is a fast-growing technology company that specializes in development of Silicon Intellectual Property (SIP), platforms and solutions for AI/ML, Flash Storage, Data Center, 5G Telecommunications, Automotive and Industrial IoT applications. The Mobiveil team leverages decades of experience to deliver high-quality, production-proven, high-speed serial interconnect SIP cores, and custom and standard form factor embedded platforms to leading companies worldwide. With a highly motivated engineering team, dedicated integration support, a flexible business model, strong industry presence through strategic alliances and key partnerships, Mobiveil solutions add value to users by matching their product goals on time and within budget. Mobiveil is headquartered in Silicon Valley with engineering development centers located in Milpitas, CA, Chennai, Bangalore and Hyderabad, in India, and sales offices and representatives located in the U.S., Europe, Israel, Japan, Taiwan and the People’s Republic of China.

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